Thermal Studies of BEOL-compatible Top-Gated Atomically Thin ALD In_2O_3 FETs

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Abstract

In this work, we investigate the thermal issues of top-gated (TG), ultrathin, atomic layer deposition (ALD) grown, back-end-of-line (BEOL) compatible indium oxide (In_2O_3) transistors by observation and visualization of the self-heating effect (SHE) using high-resolution thermo-reflectance (TR) measurement. SHE is alleviated by highly resistive silicon (HR Si) substrate with high thermal conductivity (κ_{Si}). The increased temperature (ΔT) of the devices on HR Si substrate is roughly 6 times lower than that with SiO_2/Si substrate. Furthermore, thermal simulation with a finite-element method exhibits exceptional agreement to ΔT distribution with experimental results. By thermal engineering, TG In_2O_3 transistors with channel thickness (T_{ch}) of 1.8 nm and high drain current (I_D) up to 2.65 mA/μm are achieved.

Introduction

Oxide semiconductors have been explored as promising channel materials for BEOL logic and memory applications recently [1–9], where indium oxide (In_2O_3) [1–4] and doped indium oxide [5–9] are of special interest due to their outstanding properties including homogeneous wafer-scale growth, ambient stability, high mobility, atomically smooth surface roughness, and low thermal budget BEOL compatibility for monolithic 3-D integration. On the other hand, most demonstrated In_2O_3 transistors use a back-gated (BG) design [1–3] due to the difficulty of forming a high-quality interface between the high-k dielectric layer and In_2O_3 channel, as well as SHE related thermal issues. However, for practical applications, TG devices are especially desired.

To understand and resolve the self-heating issue, in this work, an ultrafast high-resolution thermo-reflectance imaging technique is introduced to observe and visualize the SHE and temperature increase of TG In_2O_3 transistors with different substrates under different power density conditions. Moreover, thermal simulations are performed and match well with the experimental measurements. The ΔT of In_2O_3 devices with highly resistive Si (resistivity ~ 10^5 Ω·cm and κ_{Si} = 142 $W \cdot m^{-1} \cdot K^{-1}$ [10]) substrates is reduced by a factor of 6 compared to SiO_2/Si substrates. Therefore, an exceptionally high I_D of 2.65 mA/μm is achieved with 1.8-nm-thick TG In_2O_3 devices by employing HR Si as the substrate to substantially alleviate the SHE.

Device Fabrication and Performance

Fig. 1 presents the schematic diagram of TG In_2O_3 transistors. After substrate solvent cleaning, 45 nm of Ni was deposited by e-beam evaporation to form the source/drain (S/D). The 1.5–1.8 nm In_2O_3 channel was grown by ALD at 225 °C and isolated by an Ar/BCl_3 dry etch process, and the 6.4 nm HfO_2 dielectric stack was formed by ALD at 120 °C. The top gate metal of 50 nm Ni was deposited finally followed by a rapid-thermal-annealing (RTA) treatment at 200–235 °C in O_2 ambient.

Fig. 2 exhibits the transfer characteristics of a long-channel TG In_2O_3 device with channel length (L_{ch}) of 400 nm on SiO_2/Si substrate after O_2 annealing at 200 °C, showing an I_{on}/I_{off} ratio of more than 7 orders and subthreshold slope (SS) of 163 mV/dec. Fig. 3(a) shows the output characteristics of a short-channel transistor with L_{ch} of 80 nm on SiO_2/Si substrate after O_2 annealing at 230 °C. A maximum I_D of 875 μA/μm at V_{DS} of 1 V is demonstrated, exceeding the previous report of 570 μA/μm [2]. However, it is unfeasible to achieve I_D values as high as 2.2 mA/μm that have been shown with BG transistors [1] using traditional SiO_2/Si substrates, since SHE starts to degrade the device performance when larger V_{DS} is applied. As shown in Fig. 3(b), higher I_D conducts through the ultrathin channel with an enhanced V_{DS} of 1.6 V, generating a substantial of thermal energy that cannot be dissipated efficiently by the substrate. Consequently, the local temperature around the channel is drastically elevated, which damages the In_2O_3 and even HfO_2 [4].

Thermo-Reflectance Measurement and Thermal Engineering

To quantitively investigate and address the SHE, an ultrafast high-resolution TR measurement system is introduced with the setup illustrated in Fig. 4. Periodic V_{DS} pulses are applied to the device under test, and a direct-current (DC) supply provides a constant gate-to-source (V_{GS}) bias. The device is also illuminated by high-speed LED pulses, and a synchronized charge coupled device (CCD) camera is employed to capture the surface reflectance. Fig. 5 reveals the working mechanism in time domain. As a V_{DS} pulse starts/ends, the device is turned ON/OFF and therefore heated up / cooled down. After the steady-state is reached, TR signals are captured as active/passive images. This process is repeated numerous times, and the difference between the active and passive images is averaged accordingly to maximize the signal-to-noise (STN) ratio as presented in Fig. 6. The resultant image of reflectance change is transformed into a temperature scale through dividing by the TR coefficient of the surface material (C_{TH} = -5×10^{-5} K^{-1}) and calibration to obtain the final thermal image [11].

Figs. 7–9 manifest the channel region of steady-state ΔT of TG In_2O_3 devices with L_{ch} of 400 nm, W_{ch} of 2 μm, and SiO_2/Si substrate at power density of 2.44 kW/mm^2, sapphire substrate at 2.65 kW/mm^2, and HR Si substrate at 3.00 kW/mm^2, respectively. The In_2O_3 transistors have the same structure except for the different substrates in use, and the power density is calculated by ($I_D \times V_{DS}$) / ($L_{ch} \times W_{ch}$). The results show a clear correlation between increasing thermal conductivity of the substrate material and decreasing ΔT (κ_{SiO2} / κ_{sap} / κ_{Si} = 1.1 / 40 / 142 $W \cdot m^{-1} \cdot K^{-1}$ [10,12,13]). The reason is that a substrate material with better thermal conduction is able to dissipate the generated heat more efficiently. The cross-sections of Fig. 7–9 are normalized by power density and plotted in Fig. 10 for a clear comparison. The $\Delta T/P$ values for sapphire and HR Si substrates are roughly 2.7 and 6 times smaller than that for SiO_2/Si, indicating that the SHE can be mostly eliminated by utilizing HR Si as the substrate.

To verify the TR measurement results, thermal simulation with a finite-element method is carried out through COMSOL. The model design, which is similar to the discussed In_2O_3 TG transistors, and its mesh build-up are illustrated in Fig. 11. The red square in Fig. 11 denotes the area of interest, and a false-color image of the corresponding area of a fabricated device is illustrated in Fig. 12. Fig. 13 reveals the simulated result with SiO_2/Si substrate and power density of 2.44 kW/mm^2 (same conditions as Fig. 7). To compare the simulation results with the TR measurements, the area of interest in Fig. 7 is shown in Fig. 14 in a similar fashion to Fig. 13, and their cross-sections are plotted in Fig. 15. It can be seen from Figs. 13–15 that the simulation and experimental results are in excellent agreement. The ΔT values of TG In_2O_3 transistors with the three different substrates at various power conditions are plotted in Fig. 16, showing a linear relation. The slope of each line is the thermal resistance (R_T) for that corresponding case. The extracted R_T values for SiO_2/Si, sapphire, and HR Si substrates are approximately 19.6, 7.4, and 3.2 mm^2·K/kW, respectively.

With the ΔT being 6 times lower, HR Si is employed as the substrate to suppress the SHE and boost the ON-state performance of TG In_2O_3 devices. Moreover, contact resistance (R_C) can be further reduced by designing the contact regions of In_2O_3 in between the S/D and TG stacks as shown in Fig. 17. The carrier concentration at the contacts, and therefore R_C, can be modulated by V_{GS}. With a positive increase of V_{GS}, R_C is decreased down to a minimum of 0.13 Ω·mm, which is lower than the previous report of 0.24 Ω·mm without the V_{GS} modulation [4]. Fig. 18 illustrates the transfer and output characteristics of a TG In_2O_3 transistor with T_{ch} of 1.8 nm, L_{ch} of 80 nm, and HR Si substrate after O_2 annealing at 235 °C, showing an ON–OFF ratio of 3 orders and a maximum I_D up to 2.65 mA/μm. Even with such high power, the generated heat can be mostly dissipated due to the high thermal conductivity (142 $W \cdot m^{-1} \cdot K^{-1}$) of HR Si. Therefore, with the low R_C and the considerably mitigated SHE, an extremely high maximum I_D of 2.65 mA/μm is accomplished with a 1.8-nm In_2O_3 TG transistor.

Conclusion

In summary, the serious SHE limitation in TG In_2O_3 transistors is greatly mitigated by thermal management with the understanding of self-heating issue through TR measurement. By thermal engineering and R_C modulation, ultrahigh I_D of 2.65 mA/μm is achieved in a TG In_2O_3 transistor with atomically thin channel of 1.8nm. The work points out a clear route to develop BEOL-compatible high-κ materials such as ALD AlN to replace SiO_2 for 3D monolithic integration.

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Reference: [1] M. Si et al., IEEE TED, p. 1075, 2021. [2] M. Si et al., IEEE TED, p. 6605, 2021. [3] M. Si et al., IEEE EDL, p. 184, 2021. [4] P.-Y. Liao et al., IEEE TED, p. 147, 2022. [5] J. Wu et al., VLSI, p. THL.4, 2020. [6] S. Li et al., Nat, Mater., p. 1091, 2019. [7] M. Si et al., ACS Nano, p. 11542, 2020. [8] S. Samanta et al., VLSI, p. TH2.3, 2020. [9] W. Chakraborty et al., VLSI, p. TH2.1, 2020. [10] H. R. Shanks et al., Phys. Rev., p. 1743, 1963. [11] P. E. Raad et al., J. Electron. Cool., 2008. [12] T. Sadi et al., IEEE TED, p. 2892, 2006. [13] M. B. Kleiner et al., IEEE TED, p. 1602, 1996.

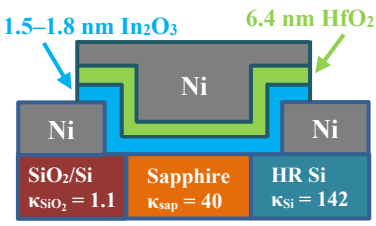


Fig. 1. Schematic diagram of TG In_2O_3 transistors with different substrates. The unit of thermal conductivity (κ) is $W{\cdot}m^{-1}{\cdot}K^{-1}$.

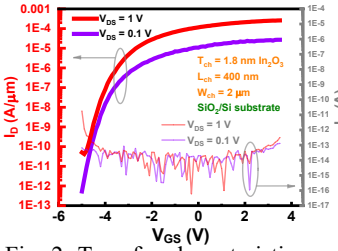


Fig. 2. Transfer characteristics of a TG In_2O_3 transistor after O_2 annealing at 200 °C with L_{ch} of 400 nm, SiO_2/Si substrate.

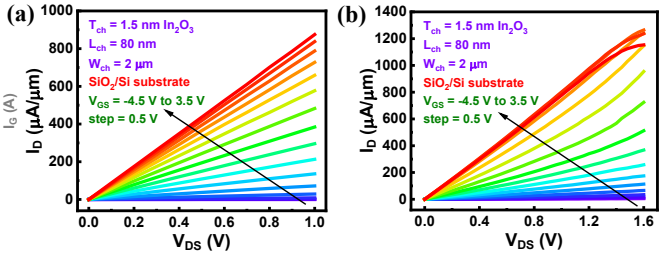


Fig. 3. Output characteristics of a TG In_2O_3 transistor after O_2 annealing at 230 °C with L_{ch} of 80 nm, SiO_2/Si substrate, and V_{DS} of (a) 1.0 V and (b) 1.6 V. The curves in (b) shows severe SHE at large V_{DS} with high I_{DS}.

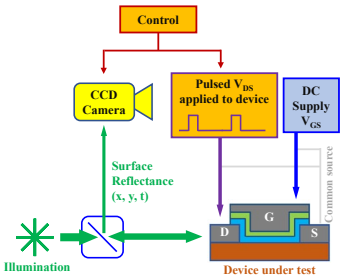


Fig. 4. Schematic illustration of the high-resolution thermo-reflectance (TR) imaging system setup.

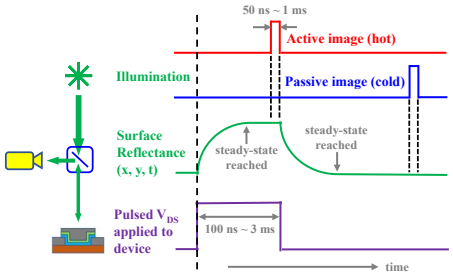


Fig. 5. Working mechanism of the high-resolution TR imaging equipment in time domain.

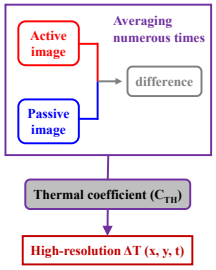


Fig. 6. Transformation from TR signal to a temperature scale.

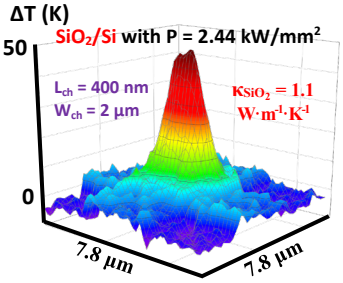


Fig. 7. Temperature increase of a TG In_2O_3 transistor with SiO_2/Si substrate and power density of 2.44 kW/mm^2.

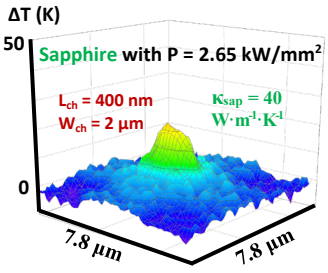


Fig. 8. Temperature increase of a TG In_2O_3 transistor with sapphire substrate and power density of 2.65 kW/mm^2.

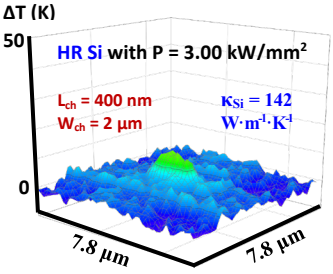


Fig. 9. Temperature increase of a TG In_2O_3 transistor with HR Si substrate and power density of 3.00 kW/mm^2.

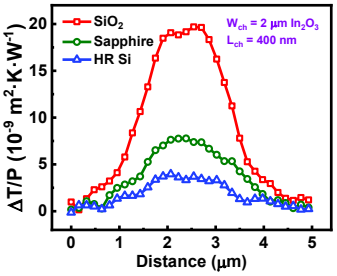


Fig. 10. Cross-sections of temperature increase of TG In_2O_3 transistors with different substrates normalized by power density.

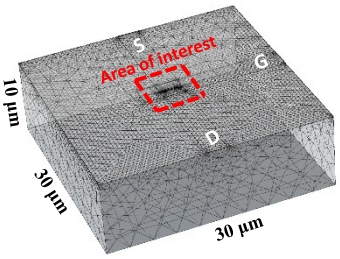


Fig. 11. Model design and mesh build-up of a TG In_2O_3 device for thermal simulation with a finite-element method.

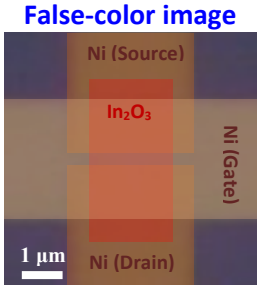


Fig. 12. A false-color image of a fabricated TG In_2O_3 device with L_{ch} / W_{ch} of 0.4 / 2 μm.

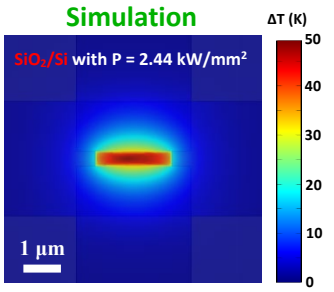


Fig. 13. Simulation result of a TG In_2O_3 device with L_{ch} of 400 nm and W_{ch} of 2 μm.

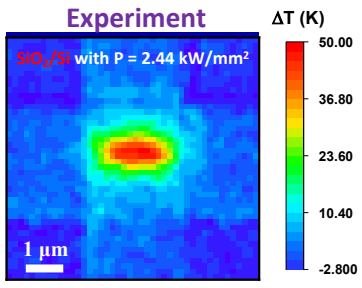


Fig. 14. TR measurement of a TG In_2O_3 device with L_{ch} of 400 nm and W_{ch} of 2 μm.

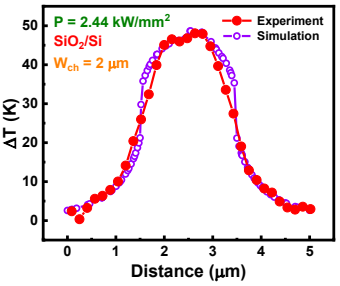


Fig. 15. Cross-sections of the simulated and experimental results of temperature increase.

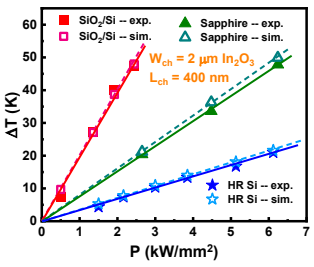


Fig. 16. ΔT extraction of TG In_2O_3 devices with different substrates and power density.

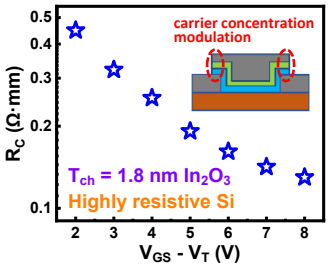
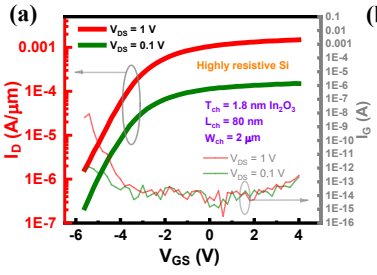


Fig. 17. R_C decreases with increasing $V_{GS}-V_T$ due to carrier concentration modulation.



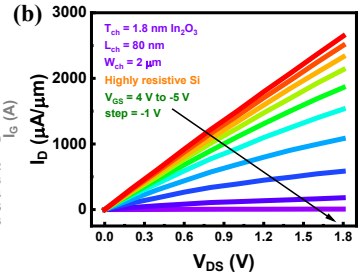


Fig. 18. (a) Transfer and (b) output characteristics of a TG In_2O_3 transistor with T_{ch} of 1.8 nm, L_{ch} of 80 nm, and HR Si substrate after O_2 annealing at 235 °C achieving maximum I_D of 2.65 mA/μm.